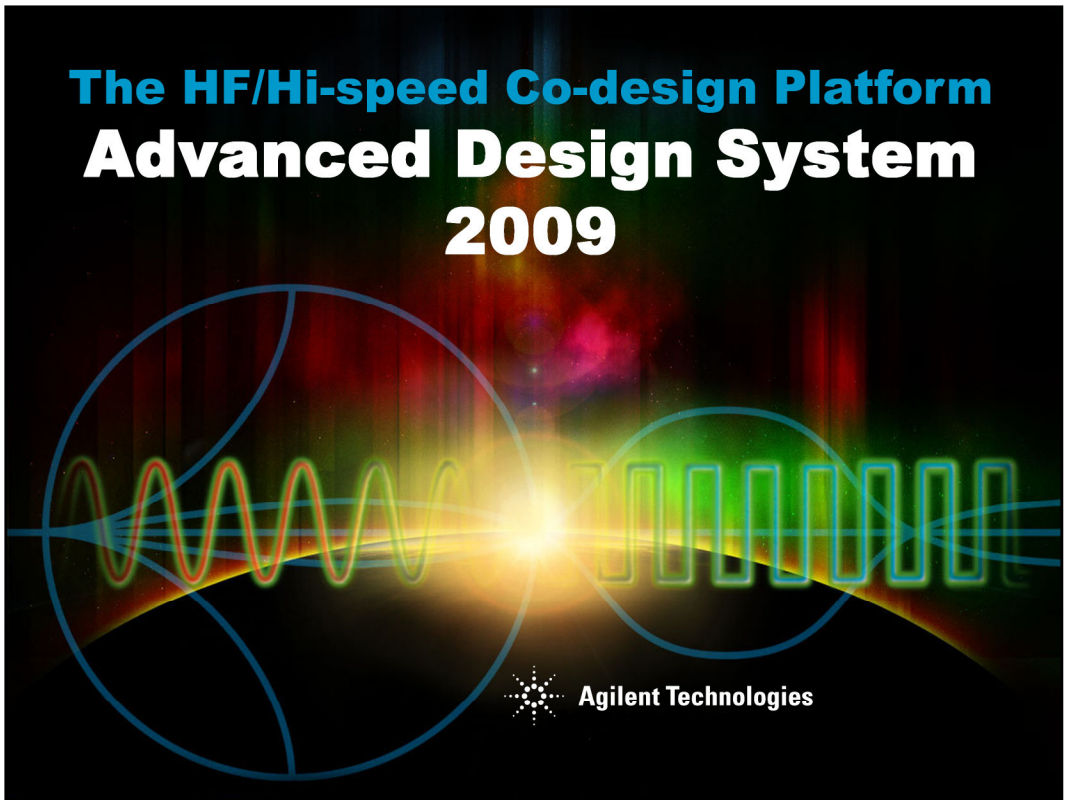
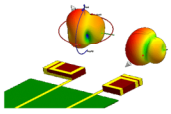


Introducing ADS 2009, the high-frequency & high speed front end co-design platform. Front-end here refers to simulation & verification platform in contrast to the backend co-design platforms from Cadence or Mentor where physical designs of the chip, package and PCB are performed.

Market pressures driving Co-Design in ADS2009

E.g. 4G LTE Smart phones- Same size, same price but need to fit

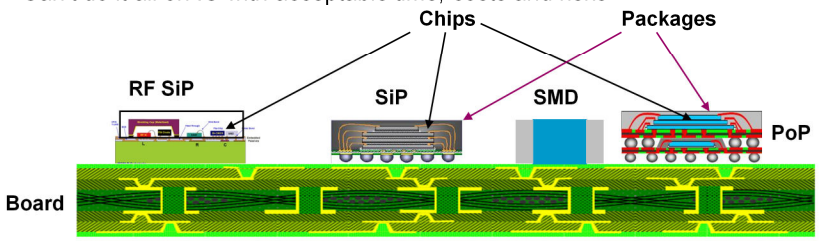
- •4G with 3G, 2G backward compatibility,
- •Bluetooth, Wifi
- •Multiband MIMO antennas



Forcing High-Frequency & H-Speed components into smaller volumes and closer proximity

Multi-technology integration-

- •Can't do it all on IC with acceptable time, costs and risks



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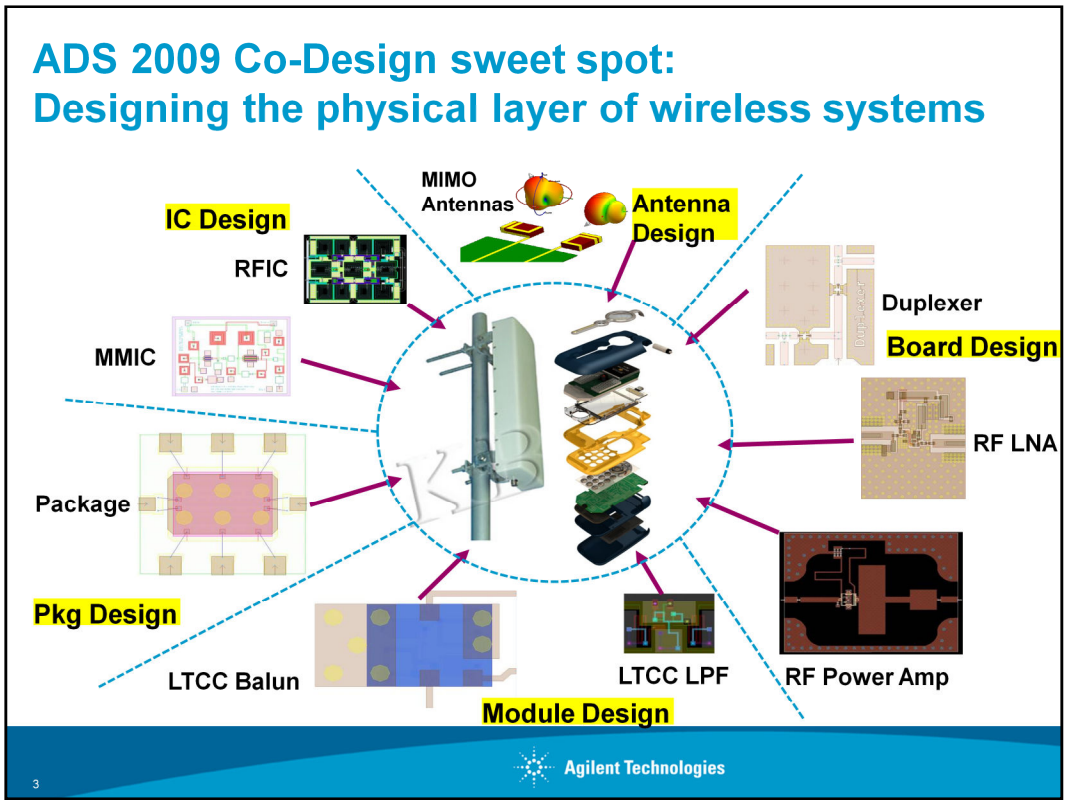
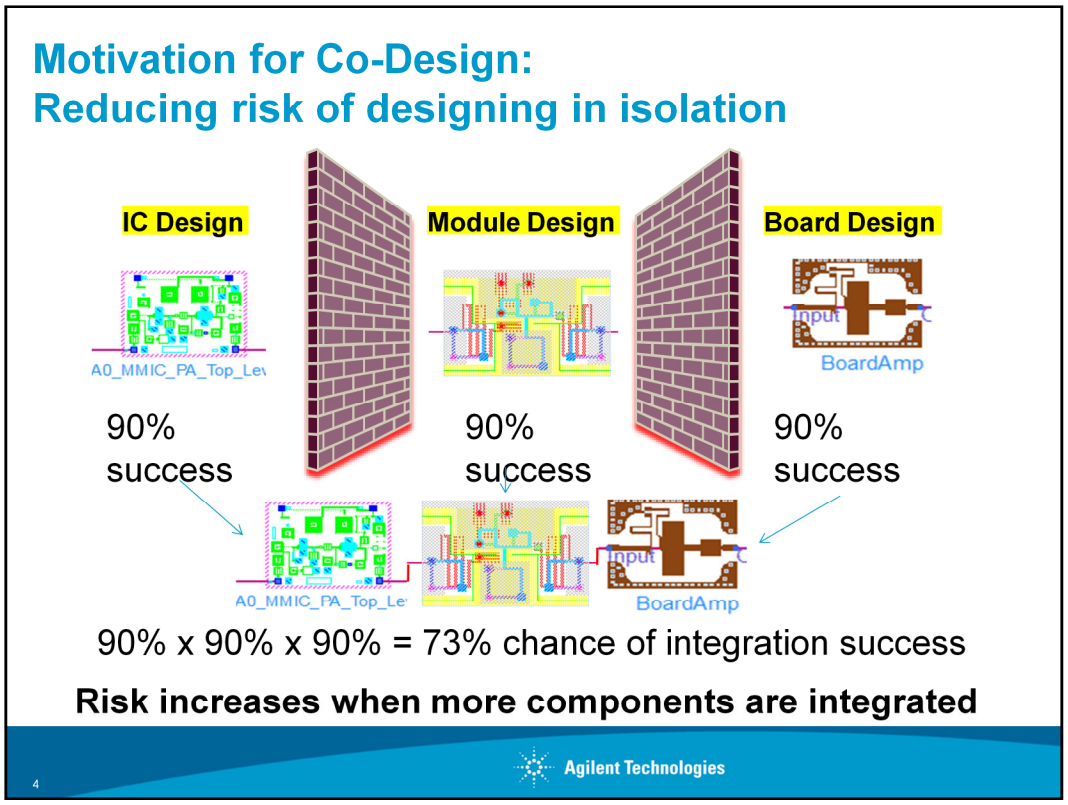
Market pressures in consumer wireless electronics are driving exponential growth in functionalities that must be integrated into the same sized and same priced packages, e.g. 4G LTE phones that must also remain backward compatible with 3G and 2G modes. These smart phones must also have Bluetooth, Wifi and MIMO capabilities which means multi-antennas operating over multi-frequency bands. These pressures force high frequency and high-speed components to be into smaller volumes and closer proximity with greater undesired interactions. Since costs & delays must be kept low, multiple available technologies are integrated onto the PCB as shown instead of designing all onto an IC.



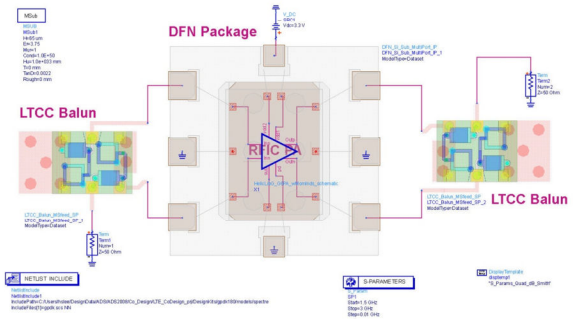
The RF physical layer of any wireless systems requires the successful integration of multi-technology components to meet the wireless systems specs such as LTE, WiMax, WiMedia, Wireless HD, etc.

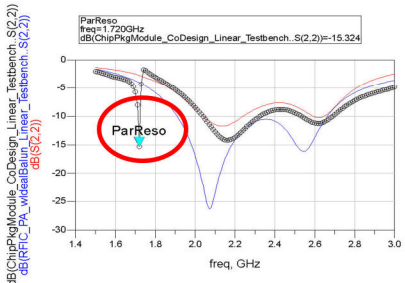


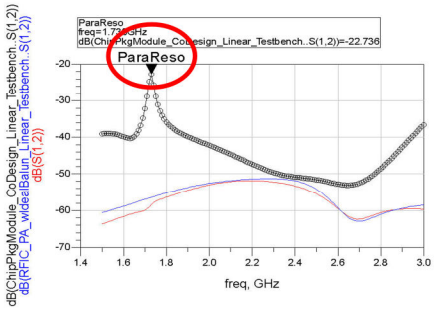
Here is a simple model to illustrate the motivation for Co-Design: Imagine your IC, Module and Board each has 90% change of success when implemented in HW. If you integrate them together when they are already in HW, the chance of success = 90% x 90% x 90% = 73%. Now if you co-design them together before fabricating HW, the chance of success for the integrated HW remains at 90%. Hence co-design reduces risk of failure by 17% in this simple case. When you extrapolate this risk reduction to a complex wireless or hi-speed communication system, the ROI is significant in the reduction of time and cost of rework. Without co-design, over-specification of components is usually done to mitigate risks, but making them more costly and more challenging to design.

Example: How ADS 2009 Co-Design prevents one failed design spin

Found unexpected resonance at 1.7GHz when integrating RFIC, Package and Balun







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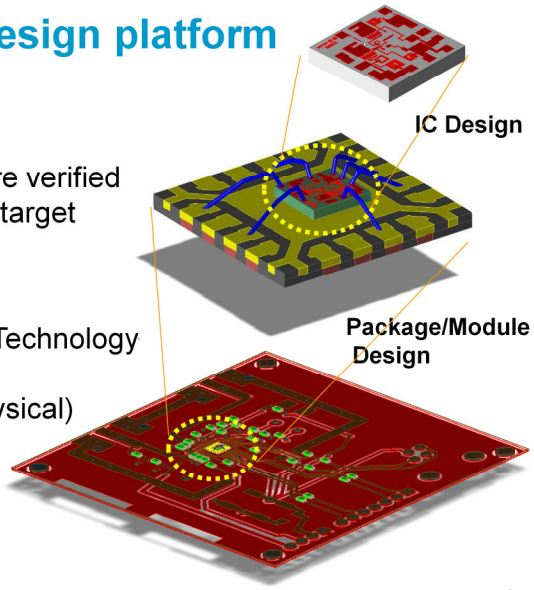
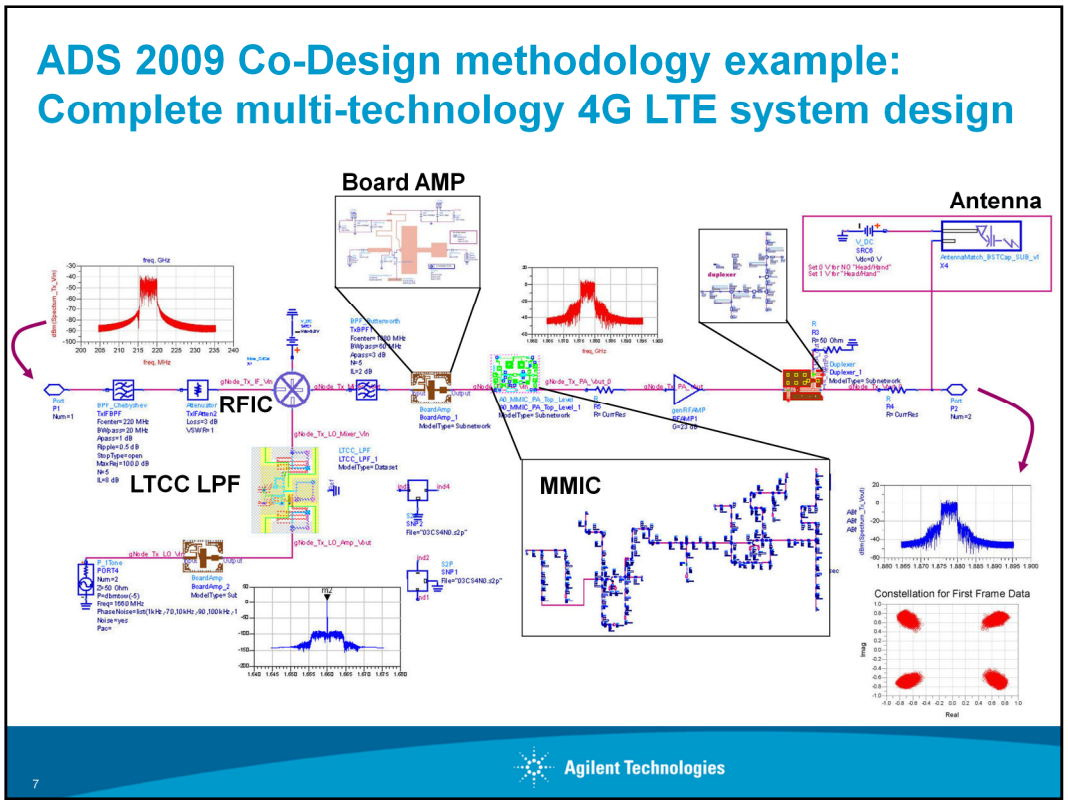
Here is an example of 3 perfectly working components: a) An RFIC power amplifier designed in Cadence and brought in as a Spectre netlist through ADS 2009 dynamic link with Cadence, b) DFN package with low loss and good impedance match, c) Balun implemented on LTCC (Low Temperature Co-Fired Ceramic). But when integrated and co-verified in ADS2009, the RFIC response was altered by unexpected resonance. This caught a failed design spin before hardware fabrication. Also shows interoperability- with Spectre netlist from Cadence.

ADS 2009 front end Co-Design platform comprises

1. Methodology:
   - Parts designed or procured are verified concurrently together against target systems specs
2. Infrastructure:
   - Simulation Platform for Multi-Technology domains (time, frequency, numeric, physical)
   - Models from measurement & simulation
   - Common system verification libraries
3. Interoperability with back-end co-design platforms from Cadence & Mentor



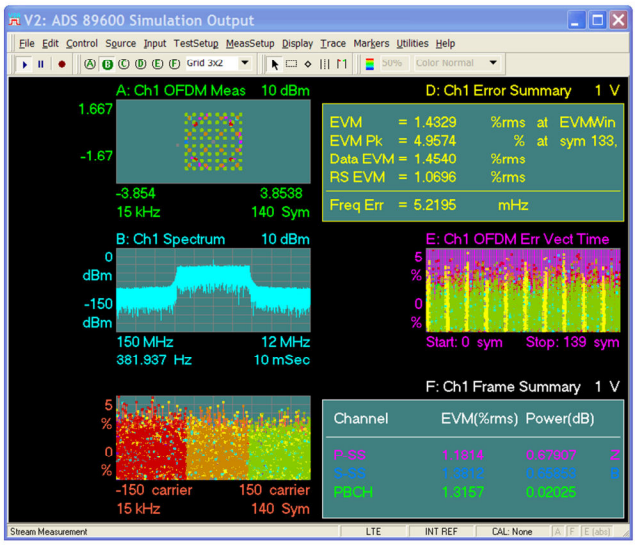
Co-Design comprises 3 important component: a) Methodology of concurrent verification of all components together against the target system specs as soon as they become available either in the form of simulated designs or actual off-the-shelf parts; b) Infrastructure that supports the front end Co-Design methodology by providing a simulation platform that supports co-simulation across multi technology domains. This means ability to combine models defined in the time, frequency, numeric or physical domains obtained through either simulation or measurements so that they can be concurrently verified by different designers using common system verification libraries; c) Interoperability with backend co-design platforms from Mentor or Cadence to complete the physical implementation.



Here is an example of implementing the front-end Co-Design Methodology in ADS 2009 with the complete multi-technology design of a 4G LTE wireless handset that comprises RFIC, MMIC, LTCC (Low Temperature Co-fired Ceramic) RF modules, PCB RF amplifier and MIMO antenna with adaptive matching for multi-band, multi-position operations.

ADS 2009 Co-Design with instrument grade accuracy for further risk reduction

Simulation and measurement share the same analysis algorithm



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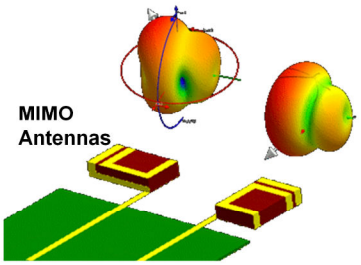
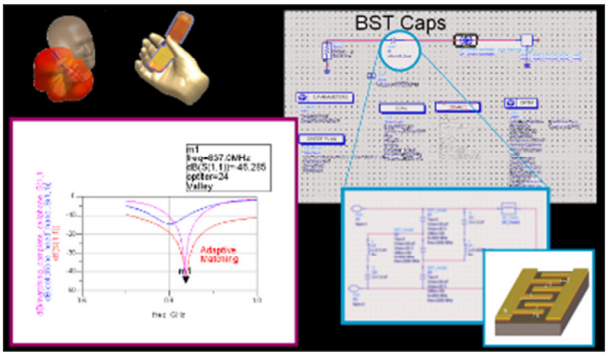
ADS 2009 employs instrument-grade accuracy in 4G LTE system verification by employing the same LTE analysis algorithms as in Agilent instrumentation. This shows the simulated LTE specs verified with Agilent's Vector Signal Analyzer which is also used when prototype or final hardware is fabricated.

ADS 2009 Co-Design includes 3DEM MIMO antenna for diversity and adaptive matching

- Exploit Multiple Reflections for Increased Bandwidth with MIMO antenna design
- Adaptive matching for phone-human positions

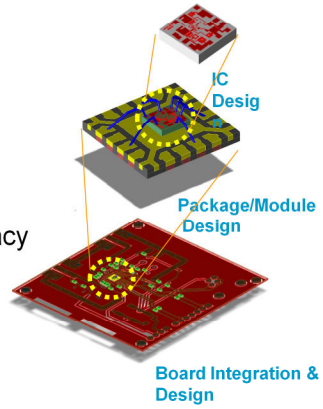




With multi antennas needed for multi-band MIMO (multiple input and multiple output) communications in LTE and WiMax, the characteristics of multi-antennas within a phone operated in various phone-human proximity positions must be taken in account for the design of adaptive antenna matching network to satisfy the LTE system performance. ADS 2009 when integrated with its companion EMPro 3DEM software enables this type of Co-Design methodology to reduce very expensive antenna and mechanical casing rework on the completed phone.

ADS 2009 front-end Co-Design infrastructure

1. Simulation platform for multi-technology
   - Faster, higher capacity multi-threaded simulators
   - Acceleration with graphics processors
   - Parallel simulation on compute clusters
   - Intelligent algorithms for increased capacity and accuracy
2. Model support for multi-technology
   - X-parameters non-linear models from measurement
   - 3D electromagnetic components for package, antennas, shields
   - Behavioral & transistor level models
   - Netlist compatibility with HSPICE and Spectre
   - Signal stimulus data to and from instruments
3. Interoperability with back-end co-design platforms from Cadence and Mentor



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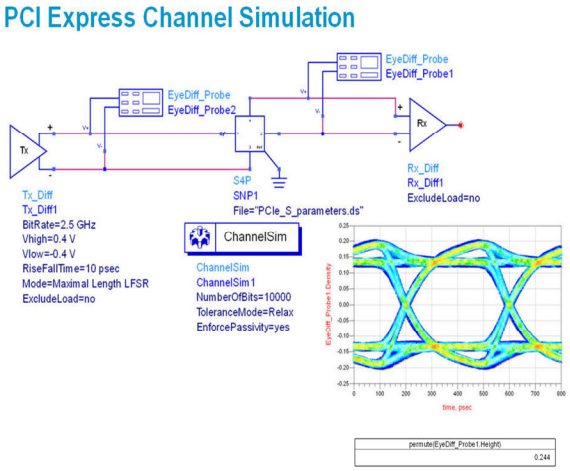
The previous section discussed the methodology of front end Co-Design. The next section presents the infrastructure in ADS2009 that supports front-end co-design: 1. Simulation platform for multi-technology – faster, higher capacity through multi-threading, acceleration, parallelism and intelligent algorithms; 2. Model support for multi-technology to accommodate accurate models from measurement of off-the-shelf parts, electromagnetic simulators, behavioral and transistor level descriptions, netlists from HSPICE or Spectre; and signal stimulus data to and from instruments; 3. Interoperability with back end co-design platforms from Cadence and Mentor

ADS 2009 introduces fast Channel Simulator for high-speed Co-Design

- New Channel Simulator
  - **1000× faster than SPICE**
  - Million-bit-per-minute throughput
  - Simulates and optimizes eye diagram opening
- New Eye Probe
  - Fast eye diagram measurements
  - Interactive what-if probing along hi-speed chip-package board channel

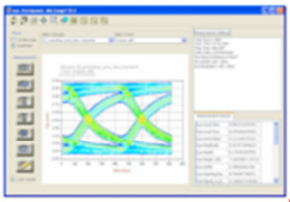


ADS 2009 introduces a new Channel Simulator for simulating and optimizing the eye diagram along any point of a high speed signal channel running over the chip-package-board interfaces. Running over 1000x faster than SPICE, it is essential ingredient for perfoming High Speed chip-package-PCB co-design.

Accelerated transient simulation with graphics processor and multi-threading

- Accelerate transient simulations 4× with massively parallel, many-core processing on NVIDIA Tesla GPU-enabled computers
- Multi-threaded impulse characterization for faster Convolution Simulator
- Jitter analysis with instrument-grade eye diagram algorithm
- Periodic & Arbitrary Jitter Analysis

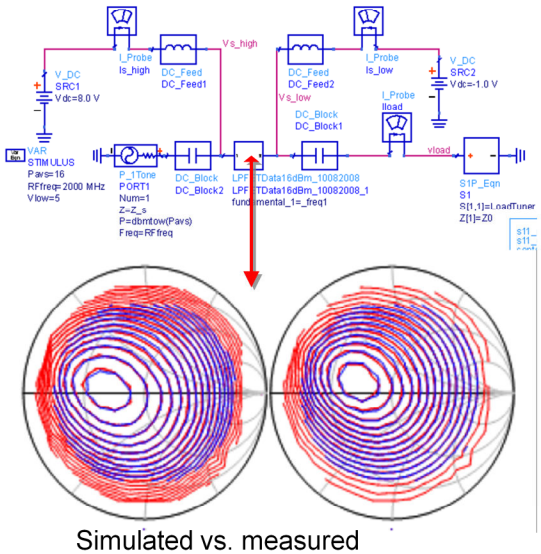
Tesla C1060 GPU accelerator from NVIDIA



Graphics processor acceleration of simulation enables faster co-design verification. In ADS 2009, the transient simulator can exploit Nvidia's latest generation of Tesla GPU (graphics processing unit) to gain 4x in speed and along with multi-threaded convolution simulator, it makes high-speed co-design a reality.

RF simulation advancements in ADS2009 for Co-Design

- **X-parameters simulation**
- Multi-threaded harmonic balance, up to 2x faster
- Support HSPICE .pat statement for complex sources
- Support for Cadence Spectre netlsts
- Synthesis of Stripline and suspended Stripline in passive design guide
- Wireless Libraries updated WiMedia v1.2, 3GPP/ LTE MIMO v8.3.0 & v8.4.0



Simulated vs. measured Power contours (left) and PAE contours (right) with X-parameter models

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RF simulation advancements in ADS 2009 include Co-Design with accurate non-linear X-parameters models from measurement, using Agilent's non-linear vector network analyzer (NVNA). The graphics on the right shows the simulated vs. measured load pull power and power-added-efficiency (PAE) contours of the X-parameter power amplifier model, demonstrating its validity over a wide range of impedance.

Other enhancements are 2x simulation speedup with multi-threaded harmonic balance simulator and compatibility with HSPICE and Spectre netlist defined sources and components for Co-Design. Also added are comprehensive passive interconnect circuit synthesis for stripline and suspended stripline components. The latest wireless standards revision to WiMedia and 3GPP LTE are also included to ensure instrument-grade system verification completeness and accuracy.

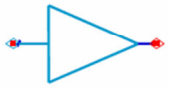
Co-Design with X-Parameters Models

Breakthrough Nonlinear Models from direct measurement

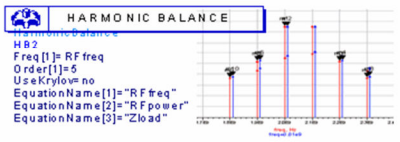
- X-parameters are mathematically correct superset of S-parameters, applicable to both large-signal and small-signal conditions, for linear and nonlinear components
- Cascadable
- Valid across wide impedance range with load pull
- You can measure, model, & simulate with X-parameters for fast and accurate non-linear RF design
- Reduces risk of failure by designing with off-the-shelf proven components

NVNA:
Measure device X-parameters

ADS:
Simulate using X-parameters



ADS:
Design using X-parameters



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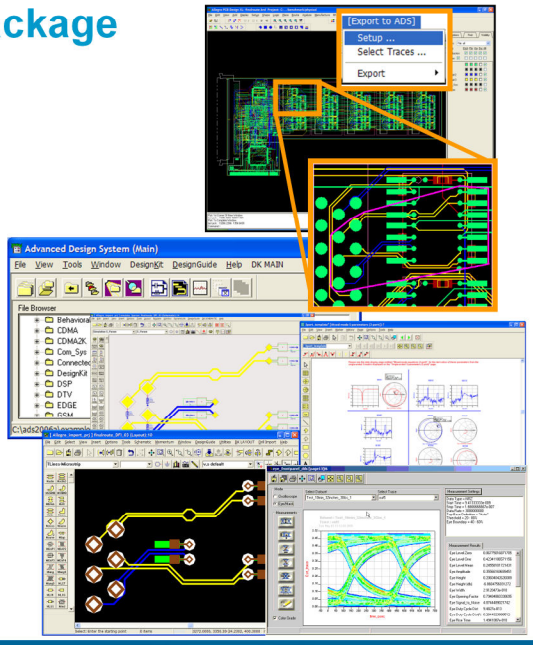
X-parameters model from non-linear measurement with Agilent's latest Non-linear Vector Network Analyzer (NVNA) is perhaps the most significant enabler for front end Co-Design in ADS 2009 because it allows off-the-shelf non-linear components such as power amplifiers or power transistors to be directly measured and used within a wireless system Co-Design. In the past, the lack of convenient non-linear models of available hardware prevents system co-design.

X-parameters are the non-linear superset of linear S-parameters and can be cascaded even with impedance mismatches to predict accurate frequency mixing and harmonics.

Interoperability with Cadence Allegro backend design flow for PCB, package and module Co-Design

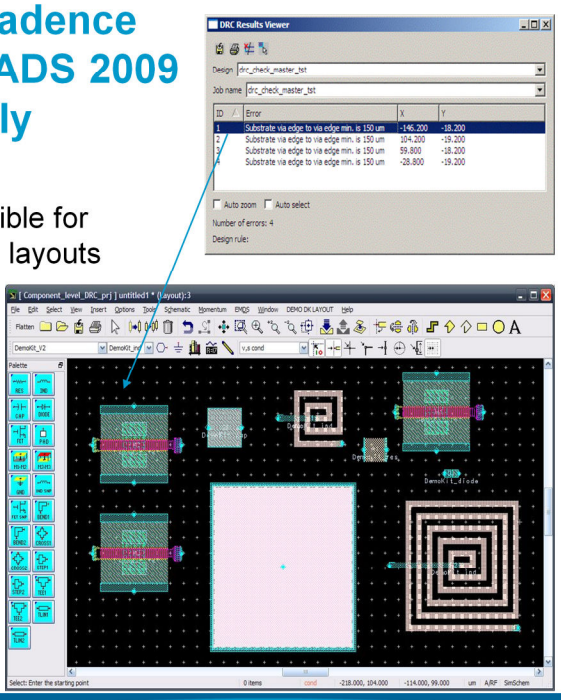
- Enhanced data transfer from Allegro
  - Imports lumped elements ,traces and vias
  - Package, PCB, and SIP artwork and schematics
- Port re-sequence for EM simulation
  - Simplifies import of critical nets from Allegro for Momentum G2 EM simulation



ADS 2009 interoperates with Cadence Allegro backend design tools: Allegro PCB, Allegro Advanced Package Designer (APD) and Allegro PCB to enable physical design to be convenient transferred into ADS for co-design with active components for optimal high-frequency and high-speed performance.

Interoperability with Cadence & Mentor DRC allows ADS 2009 to fix DRC errors locally

- DRC for Flattened Layout
  - Device level DRC now possible for both hierarchical & flattened layouts
- Integration with external DRC tools
  - Mentor Calibre
  - Cadence Assura
  - Triquint MailDRC
  - Allows ADS layout to view, edit and fix errors reported from external DRC tools



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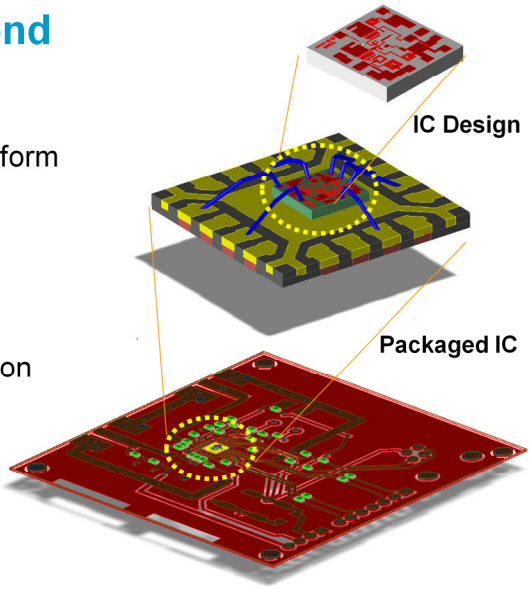
ADS 2009 interoperability with Cadence and Mentor backend design flows extend to MMIC and RFIC design rule checking. DRC violations reported by Cadence Assura or Mentor Calibre or Triquint foundry MailDRC can be directly read and fixed in ADS 2009 layout to provide a cost effective MMIC or RFIC layout solution (>4x lower cost than Cadence) that can also be incorporated with the rest of the ADS 2009 Co-Design methodology.

ADS 2009 enables front-end Co-Design with:

1. Multi-Technology Simulation Platform
   - Multi-threading
   - Acceleration
   - Channel Simulator
   - LTE, Wimax, WiMedia verification libraries
2. Multi-technology Model Support
   - X-parameters
   - 3D EM integration
3. Interoperability with backend design platforms



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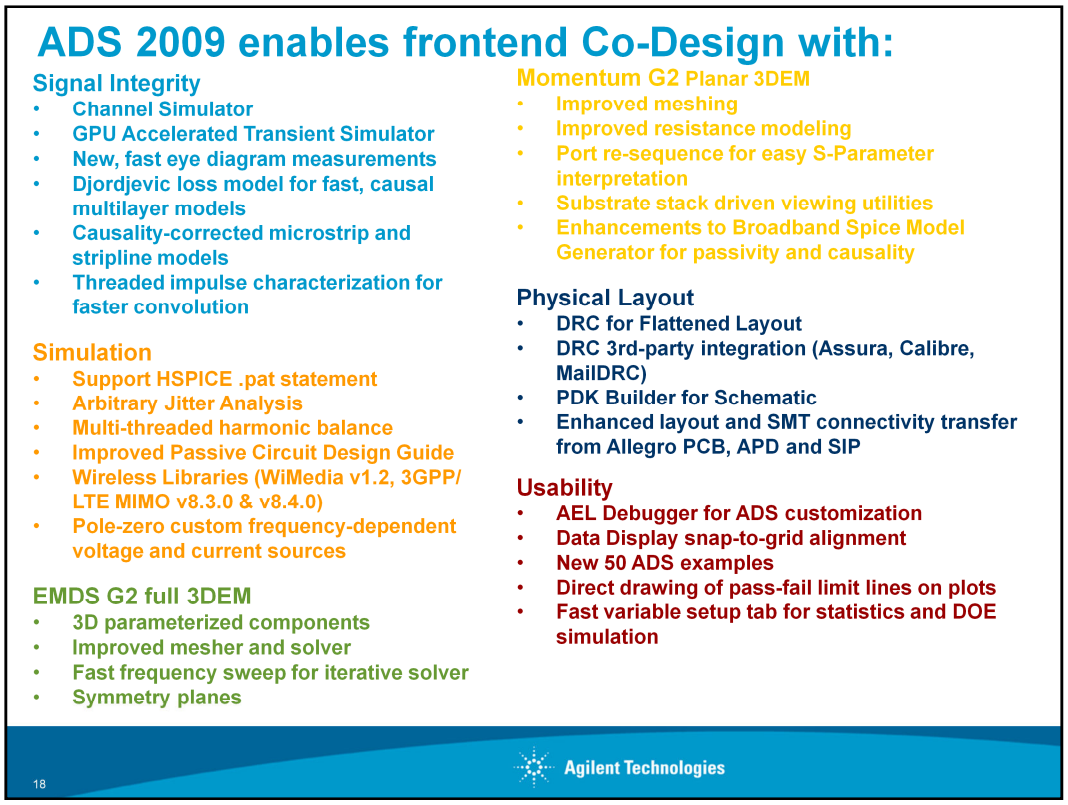
ADS2009 is a co-design platform, not a point tool, for High Frequency and Hi-Speed IC, Package, Module and Board Co-Design. It enables multi-technology components to be co-designed and co-verified against target system specs to understand their interactions that impact Signal Integrity or Wireless System performance. No other design platform on the market has a much technological depth and breath delivered with the latest Wireless Standards libraries to enable the latest high-speed and wireless applications to be Co-Designed with the minimum time, cost and risks.



These are not random accumulation of features, but a collection of synergistic capabilities build on top of an already powerful and versatile ADS platform to enable the co-design of HF/Hi-Speed IC, Package, Module & Board to minimize time, cost and risk of developing hi-speed and wireless products for today's market in a difficult economy. Only ADS protects your EDA investment for now and into the future with proven depth and breadth of technologies that you can grow with .